EXPEDITED PROCEDURE - EXAMINING GROUP 2812

PATENT

#17/Response
3/14/02
V. Vanness

SN 09/382,442

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan R. Reinberg
Serial No.: 09/382,442
Filed: August 25, 1999
Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

Examiner: Richard A. Booth
Group Art Unit: 2812
Docket: 303.522US1

RESPONSE

Box AF
Commissioner for Patents
Washington, D.C. 20231

REMARKS

Applicant has carefully reviewed and considered the Advisory Action mailed on December 14, 2001 and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-14, 26-32 and 35-39 remain pending in this application.

§103 Rejection of the Claims

Claims 1-14, 26-32, and 35-38 were rejected under 35 USC § 103(a) as being unpatentable over Applicant's admitted prior art in view of Lisenker et al. ((WO 94/19829) The Examiner has not included the Clark et al. reference in the Advisory Action comments. As has been discussed, the Lisenker et al. reference does not discuss a use of deuterium for reducing random single bit data loss in a FLASH memory cell.

The significance of this difference is that FLASH memory includes a programming operation and an erase operation. Both the programming operation and the erase operation must operate in a satisfactory manner for the FLASH memory to perform acceptably. None of the MOSFET devices, TFT's, polyresistors or polyemitter bipolars operate with this two step operation. Thus, there is no precedent in the references cited by the Examiner for concluding that deuterium substitution would work at all to reduce random single bit data loss in a memory cell. The observations described in Lisenker et al. patent suggest that deuterium treatment would not be effective in an erase operation because deuterium does not have the same removal properties